second plate electrodes, the polarization of said capacitors corresponding to the data stored therewithin, the improvement wherein:

said memory further comprising a plurality of word lines and a plurality of plate lines distinct from said bit lines and word lines, each of the memory cells being coupled to a word line, each memory cell being coupled also to a plate line, each plate line being coupled to a capacitor plate electrode of a cell; and

each said memory cell further including a respective switching device located within the memory cell, said first plate electrode of said capacitor in said cell being coupled to one said bit line via said switching device, said switching device being coupled to be controlled by one said word line, said second plate electrode of said capacitor in said cell being coupled to one said plate line.

Newly added Claims 73 and 74 correspond exactly to respective Claims 1 and 17 of the '664 patent. Newly added Claim 72 corresponds exactly to the count. The count substantially corresponds to patent Claim 1.

The patent Claim 1 corresponds to the count except for immaterial limitations of the claim. The immaterial limitation relates basically to the terminology of the rows and columns, which terminology has been excluded from the count.

In accordance with 37 C.F.R. §1.607(a)(5), the added claim corresponding to the count may be specifically applied to the Applicants' disclosure as follows:

Claim Corresponding to Count	Applicants' Disclosure
72. In a nonvolatile memory of the type having a plurality of memory cells, a bit line coupled to each said memory cell, each said memory cell comprising a ferroelectric capacitor having first and second plate electrodes, the polarization of said capacitors corresponding to the data stored therewithin, the improvement wherein:	Title, Pages 11-13; Figure 4
said memory further comprises a plurality of word lines and a plurality of plate lines distinct from said bit lines and word lines, each of the memory cells being coupled to a word line,	Page 9, Lines 29-34, Page 10, Lines 1-6; Figure 2 Page 12, Lines 13-17; Figure 4 Page 13, Lines 24-26
each memory cell being coupled also to a plate line, each plate line being coupled to a capacitor plate electrode of a cell,	Page 12, Lines 13-17; Figure 4 Page 13, Lines 26-27
each said memory cell further including a respective switching device located within the memory cell,	Page 9, Lines 20-29; Figure 2 Page 10, Lines 10-13; Figure 4
said first plate electrode of said capacitor in said cell being coupled to one said bit line via said switching device,	Page 10, Lines 10-13; Figures 2 & 4
said switching device being coupled to be controlled by one said word line,	Page 13, Lines 23-26; Figure 4
said second plate electrode of said capacitor in said cell being coupled to one said plate line.	Page 9, Lines 29-30; Figures 2 & 4

Enclosed herewith is a check in the amount of $72.00 for the new independent claims. Any additional fees for the proper filing of this Amendment, including any additional

extension fees necessary under Rule 136, should be withdrawn from Richards, Medlock & Andrews deposit account #18-1260.

Corresponding requests for interference with the same U. S. Patent are being filed concurrently in the following related patent applications:

Serial No. 582,615, filed September 14, 1990

Serial No. 377,168, filed July 10, 1989

Serial No. 443,018, filed November 29, 1989

U. S. Patent Application filed concurrently herewith, which is a continuation of Serial No. 443,018 identified immediately above.

Respectfully submitted,

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